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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/642,889 | 08/18/2003 | Hiroyasu Ito | 4041J-437DVA | 3345 |

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| EXAMINER | |
|---|---|
| VU, DAVID | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/642,889 | ITO ET AL. | |
| | Examiner | Art Unit | |
| | DAVID VU | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *16-45* is/are pending in the application.

4a) Of the above claim(s) *17,20,21 and 34-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,18,19 and 22-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *16-45* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/340020.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

# DETAILED ACTION

## Election/Restrictions

1. Applicant's election without traverse of Species V (Claims 16, 18, 19 and 22-33) on 12/21/2004 is acknowledged.

Claims 17, 20, 21 and 34-45 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12/21/2004.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 16, 18, 19 and 22-30 are rejected under 35 U. S. C. 102(b) as being anticipated by Summe et al. (US Pat. 5,366,916, herein after Summe).

Regarding claims 16, 18 and 19, Summe discloses a method of manufacturing a semiconductor, comprising steps of: forming a LDMOS device on a semiconductor wafer (fig. 11); forming a final passivation film 68 (col. 9, lines 8-16 and 40-47) that transmits ultra violet

rays on an uppermost of the basic structure. The limitation "applying a bias voltage to the semiconductor device, the bias voltage having a predetermined level voltage that can maintain the semiconductor device with turning off; and radiating ultra violet rays to the basic structure of the semiconductor device through the final passivation film after the step of applying the bias voltage" is not given any patentable weight, since this is an intended method of use limitation, as discussed above. It should be noted that the claim limitations "the bias voltage applying step applies the bias voltage between a source and a drain of the switching element" (claim 18) and "wherein the ultra violet rays radiation step radiates ultra violet rays having a band whose wave length of 253.7 nm" (claim 19) are intended use recitations.

Regarding claims 22-30, Summe discloses that the step of forming the basic structure (fig. 11) includes: forming a transistor structure, formed in a semiconductor substrate defined in semiconductor wafer, comprising a n-drain region 58, a source region 60 (n+ region 62 and p+ region 64) formed in a p-channel well layer 50 (col. 6, lines 28-38) and a gate electrode 38, formed on the semiconductor substrate, with a gate oxide film 56 (col. 7, lines 51-52) interposed between gate electrode 38 and a p-channel well layer 50, transistor structure further comprising an insulating isolation film 36/36a formed between n-drain region 58 and p-channel well layer 50, wherein gate electrode 38 is formed so that a protrusion amount onto the insulating isolation film 36a is set equal to substantially a half of a width size of the insulating isolation film 36a (fig. 11), so that a maximum electric field point in the neighborhood of a surface of the semiconductor substrate occurs at substantially the center portion of a region corresponding to the insulating isolation film 36a, when a predetermined bias voltage is applied between the source region and

the drain region, and the source region and the gate electrode are at substantially identical potential.

## *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 31 and 32 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Summe (US Pat. 5,366,916) in view of Yamaguchi et al. (US Pat. 5,777,365, herein after Yamaguchi).

Regarding claim 31, Summe discloses a method of forming a LDMOS device but fails to disclose the SOI structure. However, Yamaguchi teaches a similar LDMOS transistor having the SOI substrate formed from a supporting substrate and a semiconductor layer with an insulating

film interposed therebetween, wherein transistor structure is formed in semiconductor layer (col. 3, lines 18-57 and fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Summe by forming the SOI substrate as taught by Yamaguchi since the semiconductor device of SOI structure exhibits a excellent heat-radiating characteristic while assuring breakdown-voltage and element-isolating performance.

Regarding claim 32, Yamaguchi teaches the supporting substrate is made of semiconductor material, and the supporting substrate includes a potential fixing electrode 17 formed on its back surface (col. 3, lines 58-59) to fix a potential of the supporting substrate with a predetermined level (col. 4, lines 18-32).

4. Claim 33 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Summe (US Pat. 5,366,916)

Summe discloses a method of forming a LDMOS device (see claims 22-30 above) but fails to disclose a drain region having a P-type conductivity, a source region, formed in a channel well layer of a N-type conductivity, having a P-type conductivity. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Summe by forming a P-source/drain regions and a N-channel well layer in order to use an alternatively doped type as appropriate for a given process as is well known in the art. Switching conductivity type is well known to be obvious in the art depending on the specific types of devices being fabricated.

## Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Vu

February 12, 2005.